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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,107	04/23/2004	Toshihiko Takahashi	60188-844	7526

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EXAMINER	
GUPTA, PARUL H	

ART UNIT	PAPER NUMBER
2627	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/830,107	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Parul Gupta	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are pending for examination as interpreted by the examiner. The amendment and arguments filed on 5/8/07 were considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada, US Patent 5,870,591, in view of Applicant's admitted prior art.

Regarding claim 1, Sawada discloses in figure 32 an information memory and reproduction device comprising: a variable gain amplifier for amplifying an input analog signal to a predetermined amplitude level and outputting the amplified analog signal (532); a low-pass filter for removing a noise component of the amplified analog signal (534); an A/D convert for converting the analog signal output from the low-pass filter into a first digital signal and outputting the first digital signal (535); a digital equalizer for performing wave-form equalization to the first digital signal and outputting a second digital signal (538); a clock extraction circuit for extracting a synchronous clock signal ("optimal sampling") from the second digital signal and outputting the extracted clock signal to the A/D converter and the digital equalizer (column 49, lines 56-65); and a frequency divider (551 and 552) for dividing an output from the clock extraction circuit and outputting the divided output, wherein the clock extraction circuit outputs to the A/D

converter (535) and the digital equalizer (through elements 536 and 537) a sampling clock signal (fs) having an n times higher frequency than a frequency which defines a channel clock (where n is 2 or a larger integer than 2) (column 48, lines 18-34 explain that it is a multiple of the other frequencies, but more specific numbers are given in column 49, lines 36-51), and wherein the A/D converter performs oversampling by the input sampling clock signal (column 7, lines 7-15 and column 48, lines 18-26). Sawada does not but the admitted prior art teaches in figure 6 an amplitude information detection circuit for detecting amplitude information from the signal, generating control information from the detected amplitude information and outputting the control information to the variable gain amplifier (201). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the concept of feeding back amplitude information as taught by the admitted prior art into the system of Sawada. The motivation would be to selectively compensate reduction in signal amplitude (paragraphs 0004 and 0006 of admitted prior art) for better control of the system.

Regarding claim 2, Sawada discloses the information memory and reproduction device of claim 1, further comprising a data phase comparator for selecting one of n different sampling values contained in the second digital signal and outputting a selected sampling value to the clock extraction circuit (column 51, lines 25-55).

Regarding claim 3, Sawada discloses in column 50, line 65 to column 51, line 5 the information memory and reproduction device of claim 1, further comprising a moving average value operational unit for selecting adjacent two of n different sampling values contained in the second digital signal, performing an operation to selected two sampling

values to obtain a moving average, and outputting a sampling value as an operation result to the clock extraction circuit (done indirectly through comparator of column 51, lines 25-55).

Regarding claim 4, Sawada discloses in column 50, line 65 to column 51, line 5 the information memory and reproduction device of claim 1, further comprising a moving average value operational unit for selecting at least two of n different sampling values contained in the second digital signal, performing an operation to selected at least two sampling values to obtain a moving average, and outputting a sampling value as an operation result to the clock extraction circuit (done indirectly through comparator of column 51, lines 25-55).

Regarding claim 5, Sawada discloses the information memory and reproduction device of claim 1, further comprising a sampling value operational unit ("the inclination computing circuit") for selecting at least two of n different sampling values contained in the second digital signal, performing an addition operation, a subtraction operation or an interpolation operation to selected at least two sampling values (column 50, line 65 to column 51, line 24), and outputting a sampling value as an operation result to the clock extraction circuit (done indirectly through comparator of column 51, lines 25-55).

Regarding claim 6, Sawada discloses in figure 32 the information memory and reproduction device of claim 1, further comprising a filter (536) for removing an unnecessary signal component from an output signal from the sampling value operational unit (535), the filter being provided between the sampling value operational unit and the clock extraction circuit.

Regarding claim 8, Sawada discloses the information memory and reproduction device of claim 1, further comprising an offset control circuit for adjusting a shift from a center axis of an amplitude (phase used as an acceptable alternative to amplitude) of the analog signal so that the analog signal is located within a dynamic range of the A/D converter, the offset control circuit being provided in a previous stage of the A/D converter (column 49, lines 56-65 explains controlling sampling based on results of phase of the data in a similar manner).

Regarding claim 9, Sawada discloses the information memory and reproduction device of claim 8, further comprising: an offset detection circuit ("phase difference detector" of column 50, lines 52-61) for detecting an offset of an input analog signal ("optimal") from the first digital signal ("current") and outputting a value for a detected offset to the offset control circuit ("pulse inserting/deleting circuit" of column 50, lines 25-41); an operational circuit for improving reliability of the second digital signal (column 50, line 65 to column 51, line 40); and a binarizer circuit ("second sampling register" of column 49, lines 37-41) for performing binarization ("sampling") to the second digital signal.

Regarding claim 10, Sawada discloses the information memory and reproduction device of claim 1, wherein the clock extraction circuit includes a voltage control oscillator (column 7, lines 24-34).

Regarding claim 11, Sawada discloses the information memory and reproduction device of claim 1, wherein the clock extraction circuit includes a phase synchronous loop circuit ("phase locked loop" circuit of column 7, lines 24-34).

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada in view of Applicant's admitted prior art (AAPA), further in view of Zogakis et al., US Patent Publication 2003/0086509.

Sawada in view of AAPA teaches the information memory and reproduction device of claim 1. Sawada in view of AAPA does not, but Zogakis et al. teaches, the device further comprising a downsampling circuit for changing a frequency of the second digital signal back to the frequency which defined a channel rate. (paragraph 0025). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the concept of changing the frequency of the sampling rate down to the original frequency as taught by Zogakis et al. into the system of Sawada in view of AAPA. The motivation would be to not place harder demands on other hardware to optimize the functions of the ADC (paragraph 0025 of Zogakis et al.).

Response to Arguments

4. Applicant's arguments with respect to claim 1 have been considered but are not persuasive. Applicant contends that figure 32 of Sawada does not illustrate that any signal extraction occurs from the output of the digital equalizer of element 538. However, element 539 is a sampling register that samples signal S38, which is the output of element 538. Sampling is a type of signal extraction. Further details on the process are given in column 49, lines 18-51 and column 53, lines 25-36. Applicant also contends that Sawada does not teach a digital equalizer that operates at a higher frequency than that of a channel clock. However, the output of the clocks is the same as the applicant, meaning that this feature is inherent.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Parul Gupta whose telephone number is 571-272-5260. The examiner can normally be reached on Monday through Thursday, from 9:30 AM to 7 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on 571-272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PHG
6/12/07

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER